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Question Paper Code : 52909

B.E./B.Tech. DEGREE EXAMINATIONS, APRIL/MAY 2019.

Third Semester

Electronics and Communication Engineering

EC 6304 – ELECTRONIC CIRCUITS – I

(Regulation 2013)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Name any two techniques used in the stability of the Q point.

2. When does a transistor act as a switch?

3. Which amplifier is called as voltage follower? Why?

4. Mention the advantages of cascode Amplifier.

5. A source bypass capacitor is added to the common source MOSFET circuit. Justify.

6. Calculate the output resistance of a source-follower circuit. Given that $R_s = 0.75k\Omega$, $r_0 = 12.5k\Omega$ and $g_m = 11.3\,mA/V$.

7. Determine the 3 dB frequency of the short circuit current gain of a bipolar transistor. Consider a bipolar transistor with parameters $r_\pi = 2.6k\Omega$, $C_\pi = 2pF$ and $C_\mu = 0.1pF$.

8. Define Unity gain frequency (f_T).

9. What is active load? Mention the types of load devices.

10. Compare CMOS source follower and common gate Amplifier.

PART B — (5 × 13 = 65 marks)

11. (a) (i) Determine the Q-point values of I_C and V_{CE} for the circuit in Figure 1. Assume V_{CE} = 8 V, R_B = 360 $k\Omega$ and R_C = 2$k\Omega$. Also construct the dc load line and plot the Q-point. (8)

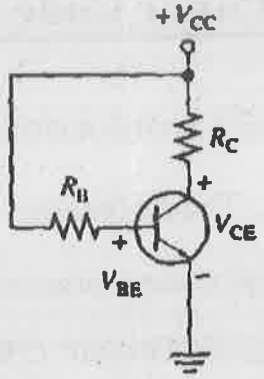

Figure 1

(ii) Explain the method of biasing the transistor using voltage divider bias. (5)

Or

(b) Design a circuit with an enhancement mode MOSFET. Consider the circuit given in Figure 2. The transistor parameters are: V_{TN} = 0.24 V, K_n = 1.1 mA/V^2 and $\lambda = 0$. Let $R_1 + R_2$ = 50 $k\Omega$. Design the circuit such that V_{GS} = 0.5 V and V_{DS} = 2.5 V. (13)

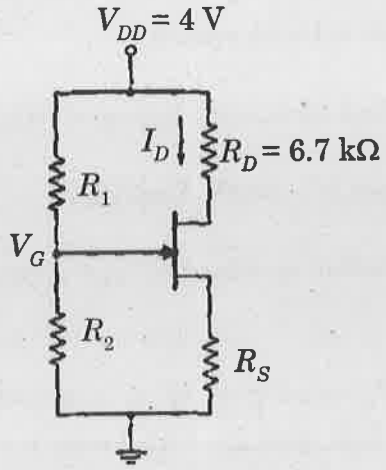

Figure 2

12. (a) (i) With relevant circuit diagrams, Explain the operation of various configurations of emitter coupled BJT differential amplifier. (9)

(ii) When the inputs to a certain differential amplifier are $V_{i1} = 0.1V, V_{i2} = -0.1V$, it is found that the outputs are $V_{o1} = -5V, V_{o2} = 5V$. When both inputs are 2V, the outputs are $V_{o1} = -0.05V$ and $V_{o2} = 0.05V$. Find the Common Mode Rejection Ratio in dB. (4)

Or

(b) Draw the circuit diagram of a Common Emitter amplifier with fixed bias, coupling capacitor and bypass capacitor. With the help of small-signal equivalent circuit, obtain the expression for voltage gain, current gain, input and output impedances. (13)

13. (a) (i) Draw the small signal equivalent circuit of common source circuit with NMOS transistor model and also obtain the expression for the small signal voltage gain of MOSFET circuit. (10)

(ii) Compare the characteristics of the three MOSFET amplifier configurations. (3)

Or

(b) Draw the small signal equivalent circuit of NMOS source follower. Also obtain the expression for the voltage gain, input impedance and output impedance. (13)

14. (a) (i) Draw the high frequency equivalent circuit of n-channel common source MOSFET circuit. Also obtain the expression for small signal current gain and unity gain bandwidth. (9)

(ii) Short circuit CE current gain of transistor is 25 at a frequency of 2MHz if f_β = 200 kHz. Calculate (1) f_T (2) h_{fe}. (4)

Or

(b) (i) Derive the expression for beta cut off frequency. (5)

(ii) Draw the small signal equivalent circuit of common emitter circuit including the equivalent Miller capacitance. Determine the Miller Capacitance. (8)

15. (a) (i) With relevant circuit diagrams, explain the working of NMOS amplifier with Depletion load. Also obtain the expression for small signal voltage gain. (7)

(ii) With relevant circuit diagrams, explain the working of NMOS amplifier with enhancement load. (6)

Or

(b) (i) Determine the small signal voltage gain of the CMOS common source amplifier given in Figure 3. Assume transistor parameters of V_{TN} = +0.8 V, V_{TP} = –0.8 V, k'_n = 80 $\mu A/V^2$, k'_p = 40 $\mu A/V^2$, $(W/L)_n$ = 15, $(W/L)_p$ = 30 and $\lambda_n = \lambda_p = 0.01V^{-1}$. Also, assume I_{Bias} = 0.2 mA. (7)

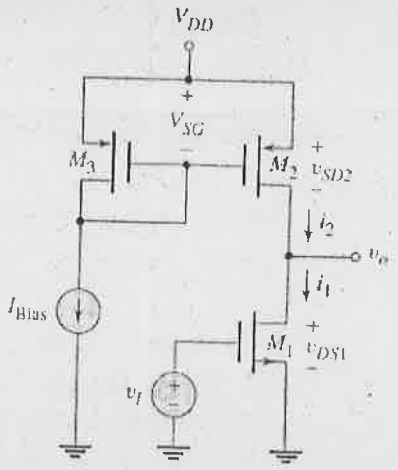

Figure 3

(ii) Determine the small signal voltage gain of the NMOS amplifier with depletion load. Assume transistor parameters of $V_{TND} = +0.8$ V, $V_{TNL} = -1.5$ V, $K_{nD} = 1$ mA/V², $K_{nL} = 0.2$ mA/V² and $\lambda_D = \lambda_L = 0.01V^{-1}$. Assume the transistors are biased at $I_{DQ} = 0.2$ mA. (6)

PART C — (1 × 15 = 15 marks)

16. (a) Design a one transistor common emitter preamplifier that can amplify a 10mV (rms) microphone signal and produces a 0.5V (rms) output signal. The source resistance of the microphone is 1 $k\Omega$. (15)

Or

(b) A MOSFET amplifier with the configuration in Figure 4 is to be designed for use in a telephone circuit. The magnitude of the voltage gain should be 10 in the midband range, and the midband frequency range should extend from 200 Hz to 3 kHz. All resistor, capacitor, and MOSFET parameters should be specified. (15)

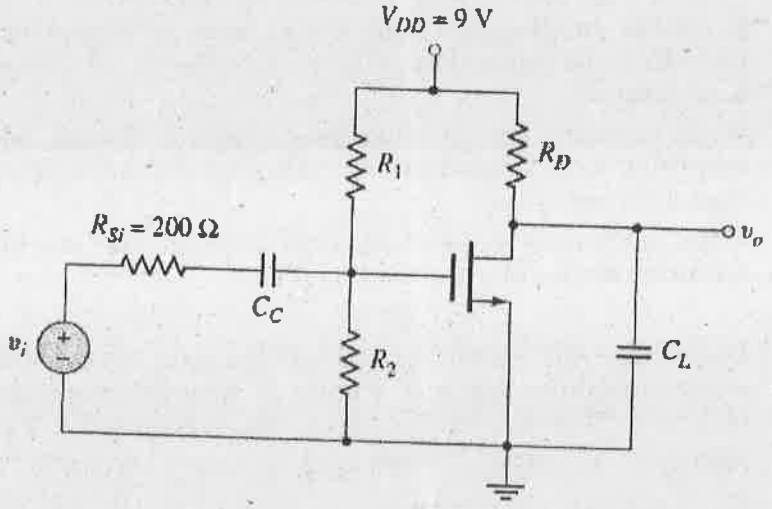

Figure 4